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A three-terminal planar selfgating device for nanoelectronic applications

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Abstract

We report on a new nanoelectronic planar three-terminal device, fabricated from III/V semiconductor-based heterosystems. Utilizing the benefits of selfgating and in-plane gates, the tunable three-terminal device presented exhibits strong non-linear input- and transfer-characteristics, both, at liquid Helium and at room temperature. For a given side-gate voltage, the devices input characteristics closely resemble that of a conventional diode, although it is fabricated by a single post-growth patterning process only, i.e., etching of deep trenches. We present a simple model, based on an equivalent circuit, which well reproduces the experimental findings. Possible applications are discussed.
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Keywords: Planar in-plane gate diode; Selfgating; In-plane gates; Nanoelectronics; Device simulation

1. Introduction

The miniaturization of conventional semiconductor devices [1] has already led to a feature size of less than 100 nm, but may soon reach its intrinsic limit. Therefore new device and circuit concepts are required. Promising candidates for future nanoelectronic devices are single electron transistors (SETs) [2–6], Y- and T-branch switches [7–17], ballistic rectifiers [18–22] or systems based on C nanotubes or InP and Si nanowires [23–27].

Another appealing approach are *in-plane gate devices*, as proposed and demonstrated by Wieck et al. [28–31]. Instead of vertical gate structures, where the conductive channel is separated form either a semiconducting or metallic gate by a dielectric layer, lateral gate electrodes are utilized. These gate electrodes consist of the same material as the active layer and are isolated from the conductive channel by either ion implantation or etched trenches extending below the two-dimensional electron gas (2DEG) of the device. Advantages of this concept are self-alignment of the gate structure with respect to the active area, few necessary lithography steps, no doped junctions required for the function of the device, small intrinsic device capacitances, allowing very high frequency operations[1] and high-input impedances, resulting in reduced power consumption and heat generation.

Selfgating processes in nanoscaled semiconductor devices have gained considerable interest in recent years.

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[1] The high frequency operating limit of the device presented here is determined by extrinsic capacitances, caused by the input leads, which may be significantly lowered by changing the layout of the input leads.

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Although mainly studied for systems in the ballistic transport regime [7,10,15,23,24], the concept can also be applied to diffusive transport [32–34].

We utilize a combination of both concepts—in-plane gates and selfgating—for the design and fabrication of a three-terminal device, which exhibits a similar input characteristics like a conventional diode, but has an in situ electrically tunable threshold voltage. These "selfgating diodes (SGD)" presented in this article are fabricated from ternary and quaternary III/V-based semiconductor heterostructures, but—because of the universality of the concept and the fact, that ballistic transport is not required—can be easily transferred into standard silicon manufacturing techniques. Especially silicon-on-insulator (SOI) based systems seem to be promising candidates, due to the good electrical isolation between different device areas by deep trench etching [35] down to the buried oxide [5,6].

2. Experimental details

The samples presented here are fabricated from two different heterostructures. Samples "A" and "B" are made from an $In_xAl_yGa_{1-x-y}As$ heterostructure [36] containing a 2DEG $t = 36$ nm below the surface. The room temperature electron density $n = 2.67 \times 10^{16}\ \mathrm{m}^{-2}$ and mobility $\mu = 0.92\ \mathrm{m}^2/\mathrm{V\,s}$ result in a sheet resistance $R_\square = 254.5\ \Omega/\square$. Sample "C" is fabricated from an $Al_xGa_{1-x}As$ based heterosystem. The corresponding parameters at liquid helium temperature (4.2 K) are: $n = 4.50 \times 10^{15}\ \mathrm{m}^{-2}$, $\mu = 1.10 \times 10^2\ \mathrm{m}^2/\mathrm{V\,s}$, $R_\square = 12.6\ \Omega/\square$ and $t = 37$ nm.

The 2DEGs of both structures are located in close proximity to the surface in order to ease the lateral patterning by wet chemical etching and to have a strong potential modulation at the 2DEG, because of short depletion lengths, allowing small structures. While the $In_xAl_yGa_{1-x-y}As$ based heterostructure is optimized for high current density operation at room temperature [37,38] (because of the low electron effective mass [39] and the high electron density), the $Al_xGa_{1-x}As$ based heterostructure is designed for very high mobility at low temperatures and is not suitable for room temperature applications, because of excessive leakage currents of the in-plane gates (IPGs) at room temperature.

A macroscopic mesa is defined using optical lithography and subsequent wet chemical etching (depth: 50 nm) using an aqueous solutions of hydrogen peroxide and phosphoric acid for the $In_xAl_yGa_{1-x-y}As$ based system and buffered hydrofluoric acid for the $Al_xGa_{1-x}As$ based system, respectively. Ohmic contacts are formed by high-vacuum deposition of Ge/Ni/Ge/Au and subsequent thermal annealing.

In the next processing step a system of trenches is defined by high-resolution electron beam lithography and wet chemical etching down to a depth of 50 nm using an aqueous solution of hydrogen peroxide and phosphoric acid, resulting in a trench width of ≈200 nm.

An atomic force micrograph of the active area of the sample is presented in Fig. 1. The source and drain contacts

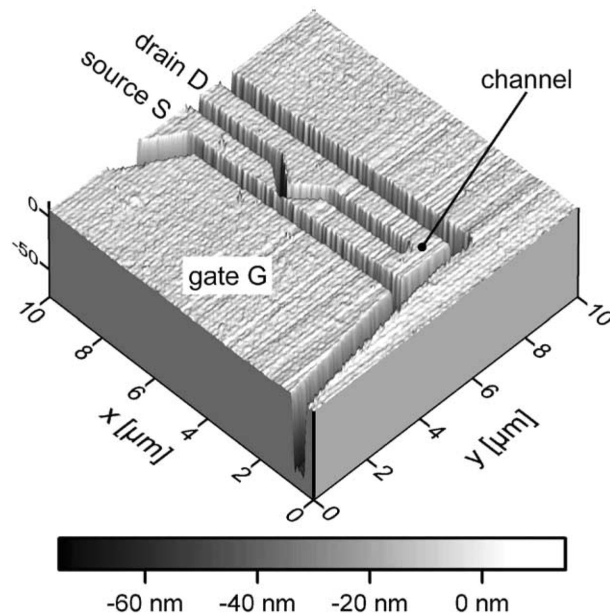

Fig. 1. Atomic force micrograph of the active device area. The width of the channel is 1 μm except for a triangular shaped constriction, where the channel is narrowed to approximately $w_{geo} = 140$ nm.

are connected via an U-shaped channel. Its width is 1 μm except at the apex of a triangular shaped constriction in the lower part of the conductive path, where the geometric width of the channel w_{geo} is reduced to approximately 140 nm. A supplementary gate electrode is located opposite to the triangle, which allows for the adjustment of the "effective electronic" channel width $w_{eff} \lesssim w_{geo}$ inside the constriction by applying a gate-voltage, resulting in a variable extend of the depletion area around the etched trench.

The devices are characterized both at room temperature using a standard analytical probing station and at liquid Helium temperature inside a ^{4}He bath cryostat, equipped with a superconductive solenoid, allowing us to apply a magnetic field up to 12.5 T perpendicular to the plane of the 2DEG. A schematic of the setup for these dc three-terminal measurements is presented in Fig. 2. The drain terminal "D" is connected to common ground and both the source–drain voltage U_{SD} applied to terminal "S" and the gate–drain voltage U_{GD} applied to terminal "G" are

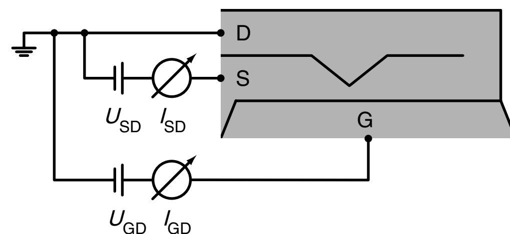

Fig. 2. Schematic of the setup for the dc three-terminal measurements. The source–drain voltage U_{SD} (applied between contacts "S" and "D") and the gate–drain voltage U_{GD} (applied between contacts "G" and "D") are both referenced to the common ground terminal. The active area of the sample, as shown in Fig. 1, is indicated in grey.

referenced to common ground. During all measurements the gate leakage current I_{GD} is carefully monitored and always is well below 1 nA.

3. Results and discussion

In Fig. 3 the input characteristics of sample "A" at room temperature is presented. The $I_{SD}(U_{SD})$-traces for different fixed gate–drain voltages U_{GD} clearly resemble a diode characteristics. The principle of operation is illustrated in Fig. 4. Here a schematic of the device is shown for different source–drain and gate–drain voltages. The etched trenches are represented by solid black lines. Due to surface states [40] inside the trenches a non-zero depletion length is present even in an unbiased situation [38,35]. These space charge regions are indicated by a grey shading. Fig. 4(a) shows the sample at zero bias. When a negative voltage is applied to the gate terminal "G", the effective channel width w_{eff} can be reduced until the channel is fully pinched-off, as shown in Fig. 4(b). When additionally a positive voltage is applied to the source terminal, the space charge region in the lower part of the U-shaped mesa is widened, so that the channel remains pinched off (see Fig. 4(c)) and only a very small parasitic current ($\approx$100 nA) can be observed as can be seen for positive U_{SD} in the input characteristics presented in Fig. 3. Although no minority carriers—like in a pn-diode—are present, the small residual current can be explained by a parasitic parallel conductive channel, i.e., via surface states [41] or via trapped electrons in the remote Si doping layer [42]. In Fig. 4(d) the forward-bias condition is illustrated, which corresponds to $U_{SD} < -1$ V in Fig. 3. The higher electrical potential in the upper compared to the lower branch of the U-shaped mesa results in a non-zero w_{eff} and a negative I_{SD}—as illustrated by the arrow—increasing rapidly with increasing absolute value of U_{SD}. As can be seen in Fig. 3, the onset voltage can be adjusted by modifying the zero-bias channel width $w_{eff}(U_{SD} = 0)$, by varying

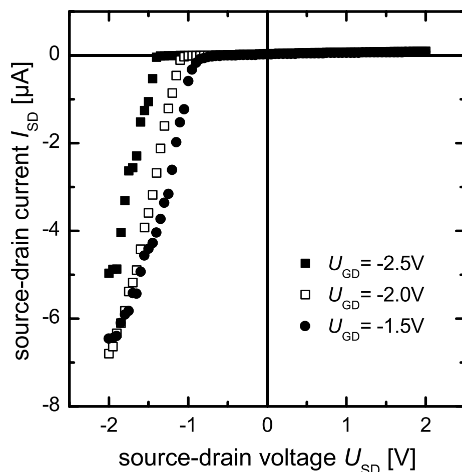

Fig. 3. Input characteristics of sample "A" at room temperature for different gate–drain voltages U_{GD}.

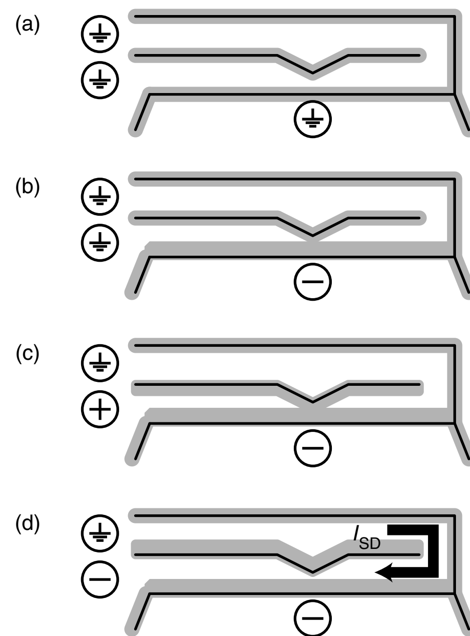

Fig. 4. Schematic view of the sample in different regimes. The black lines represent the etched trenches and the gray shaded areas illustrate the depletion zones. The effective channel width w_{eff} at the apex of the triangle determines the absolute value of the current. (a) Sample at zero bias. (b) A negative voltage is applied to the gate terminal, resulting in an increased depletion length around the gate isolation trench. Therefore the channel is pinched off. (c) Reverse-bias condition: the source electrode is positively biased, while the gate electrode is negatively biased. No current can flow, because the channel is fully pinched off. (d) Forward-bias condition: both the gate and the source electrode are negatively biased. The selfgating effect at the apex of the triangular constriction results in an increased effective channel width in comparison to (b) and a source–drain current flowing, as indicated by the arrow.

U_{GD}. The basic principle though does not rely on this additional side gate, it is used for post-fabrication fine-tuning of the device characteristics only.

To check the validity of this simple picture, we have fabricated another device (sample "B") with the same layout as sample "A" but without the triangular shaped constriction, resulting in a *symmetric* U-shaped mesa. Its input characteristics is presented in Fig. 5. As can be seen, the $I_{SD}(U_{SD})$-traces are nearly linear, indicating Ohmic behavior, which gives strong evidence for the validity of our selfgating model. Also the maximum current is nearly 50 times larger than the maximum current of the asymmetric device. From these observations one can conclude, that the two point resistance of the channel of the asymmetric sample as a whole is dominated by the resistance of the constriction and other contributions to the overall resistance like contact or series resistances can be neglected.

In Fig. 6 the input characteristics of sample "C" at the temperature of liquid Helium of 4.2 K are presented (symbols). The traces are similar to the ones obtained for sample "A" at room temperature (see Fig. 3), but are more linear in the forward-bias regime and less noise is detected. Under reverse-bias conditions the resulting source–drain current is always lower than 300 pA, which is significantly

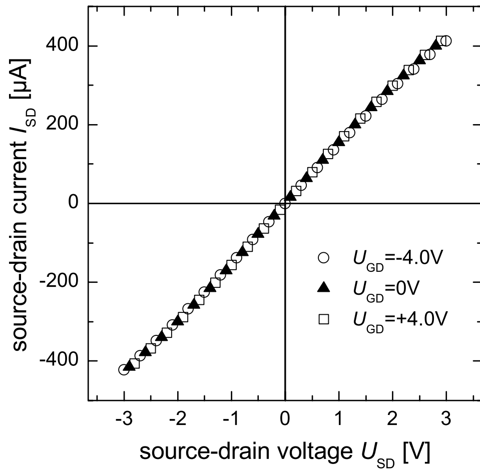

Fig. 5. Input characteristics of sample "B" (structure without a narrow constriction) at room temperature for different gate–drain voltages U_{GD}.

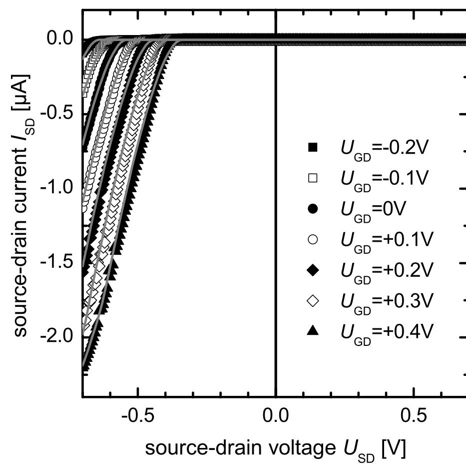

Fig. 6. Experimental input characteristics (symbols) of sample "C" at 4.2 K for different gate–drain voltages U_{GD}. The gray lines are the results of the simulation.

smaller than for the room temperature measurements of sample "A". This can be attributed to both, the sample structure and the reduced temperature. Because of the lower electron density and dopant concentration of sample "C" in comparisons to sample "A", it is very unlikely that a parallel conductive channel is present. This is further supported by the lower thermal broadening of the Fermi distribution. The absence of a parallel conductive channel is also confirmed by magnetotransport measurements of the longitudinal resistance (Shubnikov-de-Haas oscillations). The Fourier transformation indicates only a single charge-carrier density peak and therefore no parallel conductive channels. Also a linear relationship between the onset-voltage U_{SD}^{th} and U_{GD} can be observed.

The symbols in Fig. 7 represent experimental $I_{SD}(U_{GD})$-traces at different fixed negative source–drain voltages. For U_{GD} smaller than the onset gate–drain voltage U_{GD}^{th} no source–drain current can be detected, because the channel is fully pinched off. By increasing the gate–drain voltage,

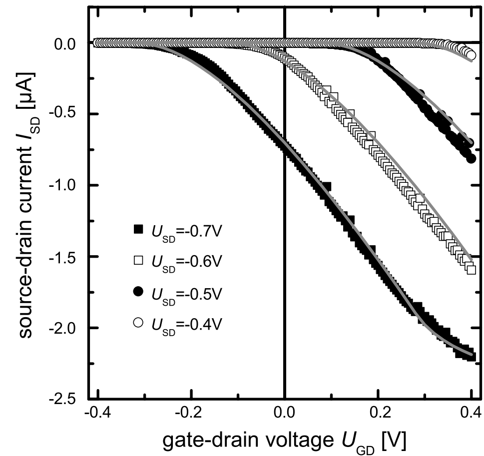

Fig. 7. Experimental transfer characteristics (symbols) of sample "C" at 4.2 K for different source–drain voltages U_{SD}. The gray lines are the results of the simulation.

the effective channel width increases, allowing a source–drain current to flow, which is rising nearly linearly with U_{GD}. At higher gate–drain voltages the source–drain current saturates. This can be explained by the fact that the effective channel width w_{eff} approaches its intrinsic limit (geometric channel width w_{geo}). This also gives evidence, that the effect of the side gate voltage is primarily due to changes of w_{eff}, rather because of changes in the charge carrier density, as utilized in conventional MOSFET or MESFET devices.

In order to get a better insight into the function of the device, we have developed an equivalent circuit diagram, which is presented in Fig. 8. The input- and transfer-characteristics were simulated using "LTSpice/SwitcherCAD III" [43]. The triangular shaped constriction is represented by an NMOS transistor, whose gate voltage is determined by the potential inside the drain line. The two resistors R_C and R_S model the resistances of the right- and left-hand side of the constriction inside the channel, while the resistance of the drain part of the channel is represented by

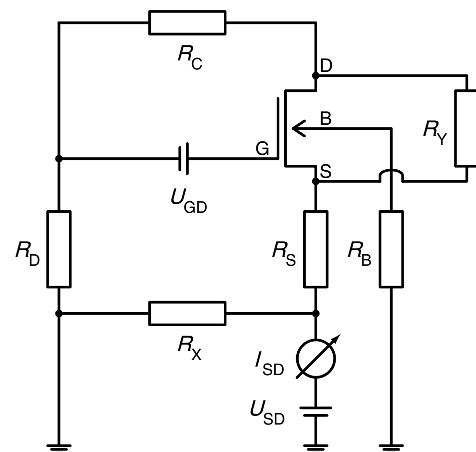

Fig. 8. Equivalent circuit diagram for the simulation.

Table 1
Various properties used for the simulation of sample "C" at 4.2 K

Element	Value
R_D	50 kΩ
R_S	10 Ω
R_C	210 kΩ
R_X	1 TΩ
R_Y	1 TΩ
R_B	1 TΩ
k_p	9.0×10^{-5} A/V^2
V_{T0}	0.54 V

R_i represent the resistances of the various resistors used, k_p the transconductance parameter and V_{T0} the zero-bias threshold voltage of the NMOS transistor.

R_D. The resistor R_X accounts for possible leakage currents between both branches of the U-shaped mesa stripe and R_Y models an unintended Ohmic parallel conductance channel inside the constriction. The substrate connector of the NMOS transistor is connected via a high-ohmic resistance $R_B = 1$ TΩ to common ground to avoid leakage currents via the substrate connector in high-imbalance situations, which would otherwise falsify the simulation. To account for the effect of the additional side gate (terminal "G" in Figs. 2 and 8) a gate–drain voltage source is inserted into the gate line. Due to screening inside the channel [11] of the samples the effective gate-voltage is only half of the value applied to the gate terminal, because the gate voltage is referenced relative to the drain terminal. This has been incorporated into the simulation by multiplying all simulated gate–drain voltages by a factor of 2 in Figs. 6 and 7. An overview of the parameters used for the simulation is given in Table 1. The parasitic resistances R_X, R_Y[2] and R_B were set to 1 TΩ, because no significant leakage current can be observed in Figs. 6 and 7, where the residual source–drain current stays below 300 pA. For the source resistance a measured value of 10 Ω was used, as determined from contact-resistance measurements. The resistance $R_D + R_C$ can be determined from the slope of the $I_{SD}(U_{SD})$-traces in the forward-bias regime for source–drain voltages, whose absolute value is slightly higher than the onset-voltage U_{SD}^{th}. The zero-bias threshold voltage V_{T0} is derived from the onset-voltage of the $I_{SD}(U_{SD})$-trace for $U_{GD} = 0$. The only two parameters remaining are the value of R_D/R_C and the transconductance parameter k_p of the NMOS transistor. They are used as fit parameters. The results are plotted as gray lines in Figs. 6 and 7. As can clearly be seen, all features for different gate voltages and both input and transfer characteristics are accurately reproduced using a single set of fit parameters. This gives further strong evidence, that the constriction of the channel at the apex of the triangle (see Fig. 1) can be considered as the source–drain channel of an NMOS transistor. The gate-voltage of this transistor is determined by the sum of the potential in the drain-line and half of the voltage applied to the lower additional side gate electrode "G" in Fig. 3. The resulting input characteristics closely resemble the characteristics of a pn-junction.

[2] The resistors R_X and R_Y are not required for the sample shown, but can be utilized to model leakage currents through different trenches inside the sample.

4. Conclusion and outlook

We have presented a new planar nanoelectronic three-terminal device, which exhibits an input characteristics, very similar to the one of a conventional diode. Additionally the onset voltage can be tuned by applying a voltage to the third terminal, allowing a very flexible application of the device, both at low temperatures and at room temperature, i.e., for efficient rectification of small signals. The principle of operation of the device utilizes two innovative techniques, namely *selfgating* and *in-plane gates*. Benefits of this design, beside low production costs are: a very simple fabrication process, high-input impedances resulting in low power consumption and heat generation and easy transferability into standard silicon semiconductor manufacturing processes. Possible applications range from simple diode or transistor devices over standard logic circuits (OR, AND, NOR, etc.), oscillators and memory cells to high-frequency switches and amplifiers [13,32,10].

The basic principle of the in-plane gate diode was explained by a simple equivalent circuit diagram, reproducing accurately both the input- and transfer-characteristics of the device.

Further improvements to the device may be achieved by using dry etching processes, i.e., reactive ion etching or plasma etching, for the fabrication of smaller feature sizes and by filling the trenches with a high-impedance dielectric material (SiO_2 or Si_3N_4) in order to reduce gate leakage currents and allowing high-current/high-voltage operations.

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